Oxidized Titanium as a Gate Dielectric for Graphene Field Effect Transistors and Its Tunneling Mechanisms

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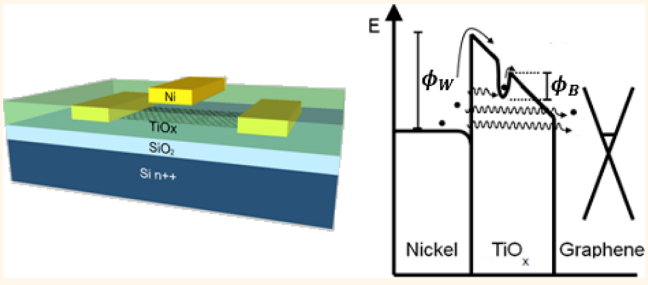
ABSTRACT We fabricate and characterize a set of dual-gated graphene field effect transistors using a novel physical vapor deposition technique in which titanium is evaporated onto the graphene channel in 10 Å cycles and oxidized in ambient to form a top-gate dielectric. A combination of X-ray photoemission spectroscopy, ellipsometry, and transmission electron microscopy suggests that the titanium is oxidizing *in situ* to titanium dioxide. Electrical characterization of our devices yields a dielectric constant of $\kappa = 6.9$ with final mobilities above 5500 $cm^2/(V\,s)$. Low temperature analysis of the gate-leakage current in the devices gives a potential barrier of 0.78 eV in the conduction band and a trap depth of 45 meV below the conduction band.



KEYWORDS: graphene · transistor · dielectric · seed layer · titanium oxide · gate leakage

Over the past decade, great strides have been made in graphene field-effect transistors (GFET): wafer scale growth,[1] dual-gated high mobility devices,[2] and large-scale integration[3,4] have been achieved. Of particular note is graphene's utility in analog RF circuits,[5] creating possibilities for ultrahigh frequency electronics.[6] These devices require high mobility and low gate leakage currents, necessitating advancements in high quality GFET gate dielectrics.[5]

While there have been many recent studies of GFETs[1−6] and graphene−dielectric−graphene heterostructures,[7−9] there are still gaps in our understanding of the surface reaction kinetics[10] and conduction mechanisms[11] through graphene gate dielectrics, and many of the physical properties of these gate dielectric materials remain unclear. The quest for novel graphene devices such as graphene tunnel FETs[12,13] will also require a greater understanding of these materials and how they affect the electrical characteristics of graphene devices. The focus of this work is to shed light on a novel physical vapor deposition (PVD) method used to fabricate the GFET top gate stack.

We study the scaling properties of oxidized titanium as a gate dielectric for GFETs. Previous work has shown that oxidized aluminum and oxidized titanium (TiO_x) can be used as a nucleation site for dielectrics deposited *via* atomic layer deposition.[2,14,15] In this study, we use only cycles of PVD of titanium and subsequent oxidation to form the gate dielectric. We fabricated a set of dual-gated GFETs with different dielectric thicknesses between 2.4 and 12 nm. Furthermore, we analyzed the gate leakage current in GFETs with TiO_x gate dielectrics as a function of temperature and electric field.

RESULTS AND DISCUSSION

We created a set of dual-gated GFETs to determine the properties of oxidized titanium as a dielectric in graphene devices. Figure 1A shows a schematic of the dual-gated GFET. To accurately determine the characteristics of TiO_x as a dielectric, a precise measurement of the oxide thickness is essential. The dielectric thickness after the cyclic deposition of the TiO_x (see Materials and Methods) was determined using a combination of ellipsometry and transmission

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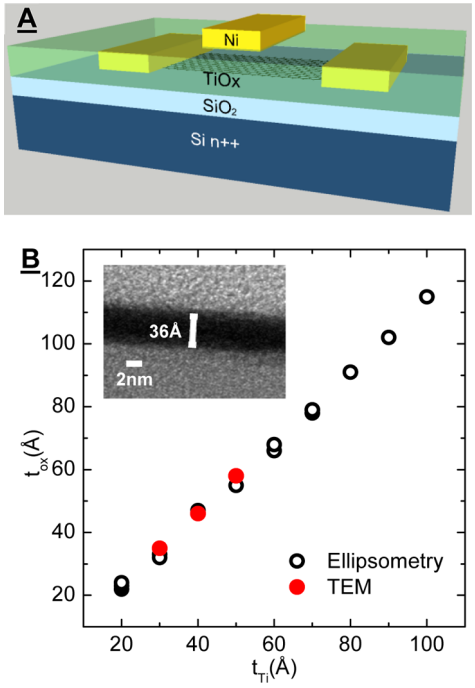

Figure 1. (A) Device schematic. (B) Measured t_{ox} as a function of t_{Ti} for all devices obtained *via* ellipsometry and TEM. Inset: TEM image of the TiO_x on the graphene channel.

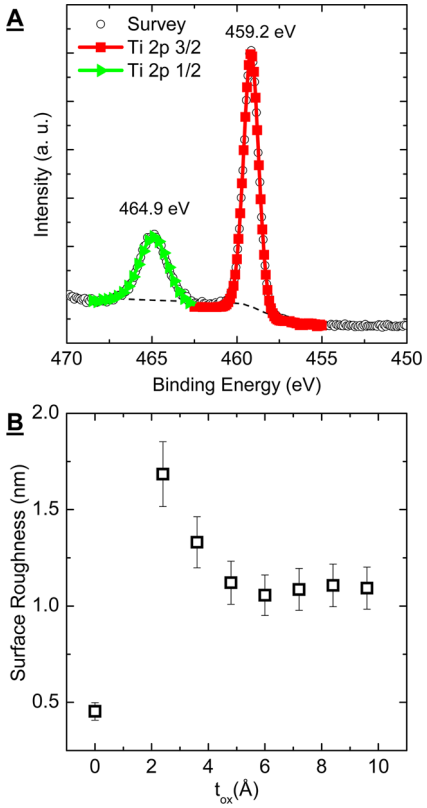

Figure 2. (A) XPS spectra of 8.4 nm TiO_x on a Si control sample. Each of the 2p bonding states shows a single Gaussian peak indicating pure TiO_2. (B) Measured R_s as a function of t_{ox}.

electron microscopy (TEM). For every fabricated GFET created in this work, a control Ti-on-Si sample was processed in parallel to measure the dielectric thickness by ellipsometry. In addition, cross-sectional TEMs were taken for several graphene devices to determine the thickness of the TiO_x on the graphene active area as compared to ellipsometry measurements of the silicon substrates. Figure 1B gives the deposited Ti film thickness (t_{ox}) *vs* the measured oxide thickness (t_{ox}) from ellipsometry and TEM. The inset of Figure 1B shows a cross-sectional TEM of three cycles of TiO_x on the graphene channel. For every 10 Å of titanium deposited on the bare silicon substrates, 11−12 Å of oxidized titanium is produced. TEM data were obtained for three GFETs with different TiO_x thicknesses, all showing a dielectric thickness within 3 Å of ellipsometric measurements on the silicon controls.

The composition of the TiO_x was also investigated with X-ray photoemission spectroscopy (XPS) on the Si control substrates. Figure 2A shows the number of electrons *vs* the binding energy of the electrons collected in the area around the Ti 2p bond states. There are two distinct peaks at 459.2 and 464.9 eV, representing the Ti 2p 3/2 and Ti 2p 1/2 states, commonly associated with titanium dioxide TiO_2.[16] The peak broadening of the Ti 2p 3/2 state in XPS measurements associated with other forms titanium oxides[17] was not present. Additionally, TiO_2 formed with similar methods has been found to be the rutile phase.[18] The rutile phase of TiO_2 has a bond length of 1.98 Å and bond angles of 81° and 91°, yielding a unit cell *z*-height of 2.96 Å.[19] The oxidation of Ti to TiO_2 would cause the as-deposited Ti film to grow, at a minimum, to three times its deposited thickness. However, the deposited film only increases in thickness by ~10% per cycle, suggesting that the evaporating titanium is oxidizing primarily *in situ* rather than in ambient. This finding suggests that the residual oxygen in the e-beam evaporation chamber, combined with the low deposition rate allows for oxidation during the Ti deposition.

Additionally, the surface roughness (R_s) as a function of oxide thickness was studied. Figure 2B shows the surface roughness of the graphene channel as a function of t_{ox}. Graphene channels after annealing had a R_s < 0.5 nm, increasing to ~1.6 nm for the thinnest working t_{ox} and leveling at ~1.1 nm above 4.8 nm. There was a 10% variation in R_s for similar thicknesses depending on the device studied.

Figure 3A shows a dual-gated GFET channel resistance (R) measured as a function of the top gate voltage (V_{TG}) at different back-gate voltages (V_{BG}) for 4.8 nm TiO_x. The inset of Figure 3A shows the V_{TG} value at the charge neutrality point ($V_{TG,Dirac}$) as a function of V_{BG}. $V_{TG,Dirac}$ has a linear dependence on V_{BG}, with a slope equal to the ratio of the back-gate (C_{BG}) to top-gate capacitance (C_{TG}). The C_{BG} values are measured using 100 × 100 μm^2 metal pads on the SiO_2 back-gate

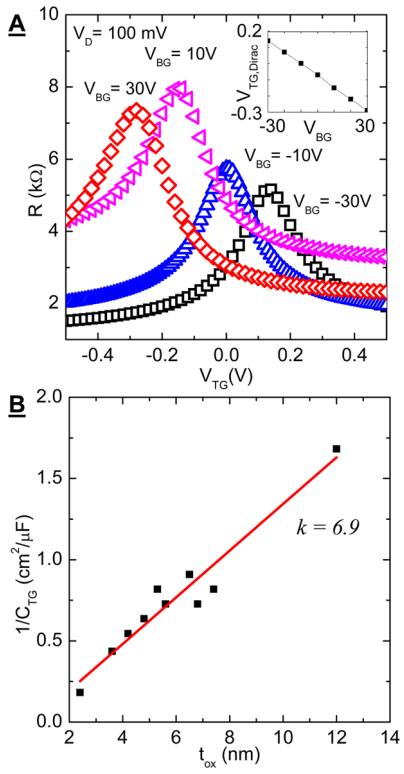

Figure 3. (A) *R vs* V_{TG} measured in a dual gated graphene FET at different V_{BG}. The 4.8 nm TiO_x top dielectric was deposited with repeated deposition of titanium and subsequent oxidation. The inset gives $V_{TG,Dirac}$ *vs* V_{BG} measured from the *R vs* V_{TG} traces. The slope of the line corresponds to C_{BG}/C_{TG}. (B) C^{-1}_{TG} *vs* t_{ox} for dual-gated graphene FETs with TiO_x dielectrics. The κ-value of TiO_x is 6.9 represented by the slope of the fitted line.

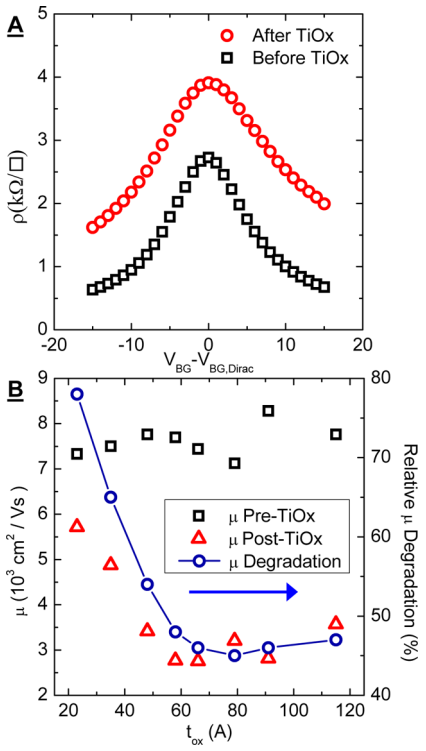

Figure 4. (A) ρ *vs* $V_{BG} - V_{BG,Dirac}$ before and after deposition of 2.4 nm of TiO_x. The mobility was 7400 and 5800 cm^2/(V s) before and after deposition, respectively. (B) μ *vs* t_{ox} for devices with varying TiO_x gate dielectric thicknesses. Data points that are vertically aligned represent a single device, *i.e.*, mobility of FETs indicated by squares degrade to those indicated by triangles after Ti deposition. The blue line (right axis) represents the relative degradation of the devices.

dielectric in close proximity of the GFET, and are independently measured with values of 8−13 nF/cm^2. Using these values of C_{BG} and the ratio of C_{BG}/C_{TG}, the C_{TG} value is calculated for each dual-gated GFET. Figure 3B shows the inverse of the capacitance per unit area (C^{-1}_{TG}) *vs* the physical thickness of the TiO_x. The data are extracted from over ten devices with various thicknesses. C_{TG}^{-1} has a linear dependence on t_{ox}, the slope indicating a TiO_x κ-value of 6.9. The *y*-value intercept of the C_{TG}^{-1} *vs* t_{ox} dependence is zero, within experimental error.

Figure 4A shows the resistivity (ρ) as a function of V_{BG} centered around the charge neutrality point ($V_{BG,Dirac}$) for a device before and after 2.4 nm of TiO_x was deposited on the channel. The device mobility (μ), extracted using the model of Kim *et al.*,[2] is 7300 cm^2/(V s) before deposition, and 5700 cm^2/(V s) after the TiO_x was deposited. All devices showed a ∼25% increase in mobility at 77 K, consistent with previous reports.[14] Figure 4B gives μ before and after TiO_x deposition for various values of t_{ox}. The initial μ value degrades after TiO_x deposition for all values of t_{ox}. The line connecting the points between different t_{ox} values represents the relative μ degradation of each device as a function of t_{ox}. Devices with similar starting μ are chosen to help clarify the effects of dielectric deposition on the electrical characteristics of the GFETs. The initial μ degradation is rapid at small t_{ox} values, but levels off, at ∼50% of the initial starting value for t_{ox} > 50 Å. These measurements are similar to previous studies of the graphene channel mobility dependence on dielectric thickness where mobility degradation was attributed to scattering from oxygen vacancies in the dielectric layer.[14,15] Additionally, oxygen vacancies in TiO_2 are known to be prevalent and could form filaments and parallel conduction pathways when biased appropriately as with resistive switching RAM.[20−22] Further studies in mobility degradation mechanisms in top-gated GFETs will be the attention of future work.

The gate leakage current density (*J*) from the graphene channel to the top gate electrode through the TiO_x was measured, and the data compared with different models to try to elucidate dominant leakage mechanisms. We indicate possible gate dielectric conduction mechanisms in our GFETs in Figure 5A, with the corresponding equations shown below. Four mechanisms might determine the leakage through the gate dielectric. The first is thermionic emission,[23] in which carriers are thermally excited over the tunnel barrier at the electrode-dielectric interface. The

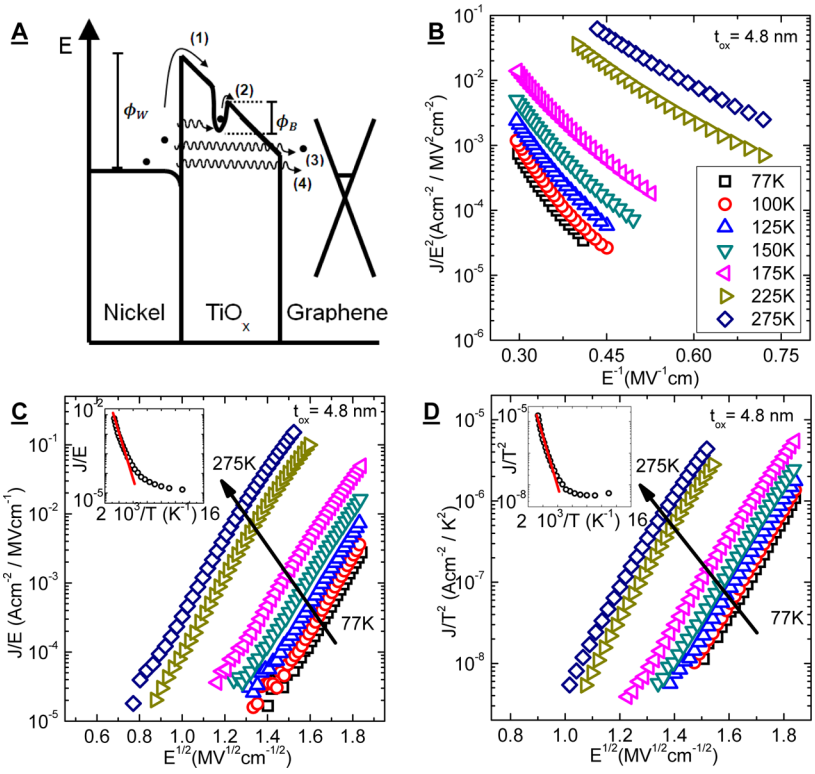

Figure 5. (A) Energy band diagram schematically showing (1) thermionic emission, (2) Poole-Frenkel tunneling, (3) Fowler-Nordheim tunneling, and (4) direct tunneling. Solid arrows represent a thermal excitation, while wavy lines represent a tunneling process. Diagram is not to scale. (B) Fowler-Nordheim plot showing J/E^2 *vs* E^{-1}. Decreasing slopes at higher temperatures may be indicative of thermally activated processes. Relatively low negative slope at low fields (right) may be indicative of trap-assisted tunneling processes. (C) Thermionic emission plot showing J/T^2 *vs* $E^{1/2}$. Inset shows J/T^2 *vs* 1000/*T* at constant E = 1.85 MV/cm. Red line intercept gives ϕ_B = 42 meV. (D) Poole-Frenkel plot showing J/E *vs* $E^{1/2}$. Inset shows J/E *vs* 1000/*T* at constant E = 2.04 MV/cm. Red line intercept gives ϕ_W = 0. 78 eV. Temperature symbols in (B−D) are the same. *Y*-axis units for the insets of (C) and (D) are the same as the parent figure.

thermionic current density (J_{TH}) has the following dependence on temperature (T), and electric field (E):

$$J_{TH} \propto T^2 \cdot \exp\left[\frac{-q}{k_B T}\left(\varphi_W - \sqrt{\frac{qE}{4\pi\varepsilon}}\right)\right] \quad (1)$$

where q is the electron charge, k_B is the Boltzmann constant, ϕ_W is barrier height between the metal and the TiO$_x$, and ε is the dynamic permittivity. The second mechanism is Poole-Frenkel[23] in which electrons tunnel into dielectric trap states, and then are thermally excited into the channel. In this scenario, the current density (J_{PF}) depends on E and T as follows:

$$J_{PF} \propto E \cdot \exp\left[\frac{-q}{k_B T}\left(\varphi_B - \sqrt{\frac{qE}{4\pi\varepsilon}}\right)\right] \quad (2)$$

where ϕ_B is the trap depth. The current density (J_{FN}) resulting from tunneling through the triangular potential barrier[21] (Fowler-Nordheim tunneling) has the following dependence on E:

$$J_{FN} \propto E^2 \cdot \exp\left(\frac{-4}{3}\frac{\sqrt{2qm_{ox}}}{\hbar}\frac{{\varphi_W}^{3/2}}{E}\right) \quad (3)$$

where m_{ox} is the mass of the carrier in the dielectric and $\hbar$ is Planck constant. Finally, the current density (J_{DT}) resulting from direct tunneling through the potential barrier[23] has the following dependence on E:

$$J_{DT} \propto \frac{E^2}{\varphi_W \beta_1} \exp\left(-\frac{2\beta_2\sqrt{2qm_{ox}}}{\hbar}\frac{{\varphi_W}^{3/2}}{E}\right) \quad (4)$$

where J_{DT} is the direct tunneling current density, β_1 and β_2 are unit-less correction terms depending on ϕ_W and E, and m_{ox} is the effect mass of the carrier. ϕ_W is determined by the difference in the nickel Fermi energy ($E_{F,Ni}$) and the electron affinity of the TiO$_2$ (χ_{TiO2}). Given that $E_{F,Ni}$ is 4.6 eV and X_{TiO2} is 3.9 eV,[24] we expect ϕ_W to be approximately 0.5 eV.

The J values were experimentally determined by biasing the graphene layer at 0.1 V between the source and drain electrodes, and varying the top-gate electrode bias from −1.5 to 1.5 V, while keeping V_{BG} at 0 V. To assess the Fowler-Nordheim and direct tunneling mechanisms in Figure 5B, we plot J/E^2 as a function of E^{-1} on a semi-log plot at multiple temperatures. In devices with low dielectric thickness, Fowler-Nordheim tunneling is characterized by a temperature independent negative slope at high E, while direct tunneling is indicated by a temperature independent positive slope at low E.[23,25] In our devices, we find strong temperature dependence for T > 125 K, indicating

thermally activated processes occurring at elevated temperatures. The positive slope of J/E^2 at low E expected for direct tunneling was not seen in any of our devices. Instead, we observed a slow decrease in slope with decreasing field consistent with trap-assisted tunneling.[26]

At high fields and low temperatures, the data is consistent with Fowler-Nordheim tunneling. Using eq 3 and the high-field slope of $\ln(J/E^2)$ *vs* E^{-1} at 77 K, we experimentally determine $\phi_W = 1.0$ eV. We assumed the tunneling effective mass in TiO_2 to be the electron rest mass. However, we note that the effective mass in TiO_2 has been reported to range between 0.7 and 14 m_0.[27]

To probe the role of the thermionic emission, in Figure 5C we show J/T^2 *vs* $E^{1/2}$ on a semi-log plot at various temperatures. Figure 5C inset is a semi-log Arrhenius plot of J/T^2 at a fixed E = 2 MV/cm. In the parent figure, thermionic emission is characterized by a linear slope of the J/T^2 on $E^{1/2}$. In the inset, this conduction mechanism is shown by the magnitude of J/T^2 being linearly dependent on T^{-1} at a constant E. In these devices, we find the slope of J/T^2 to be linear with respect to $E^{1/2}$. At constant E, there is a nearly linear dependence of J/T^2 at $T > 150$ K with a weak or no dependence at lower temperatures. Using eq 2, we are able to experimentally determine ϕ_W from the y-intercept of the linear Arrhenius dependence of J/T^2 at constant E and $T > 150$ K. In this temperature regime, ϕ_W was 0.75−0.80 eV when calculated from E = 1.9−2.1 MV/cm. The discrepancy between the ϕ_W found in the low temperature J_{FN} regime and the high temperature J_{TH} can be attributed to the uncertainty in the effective mass.

To analyze Poole-Frenkel mechanism, in Figure 5D we plot J/E *vs* $E^{1/2}$ at various temperatures. The inset gives a semi-log Arrhenius plot of J/E at constant E = 1.85 MV/cm. The main panel data shows a linear $\ln(J/E)$ *vs* $E^{1/2}$ dependence, consistent with Poole-Frenkel tunneling. Figure 5D shows that the magnitude of J/E has an exponential dependence on T^{-1}, at constant E. Using eq 2, we extract ϕ_B to be 30−70 meV for E = 1.75−1.9 MV/cm. Trap depths in polycrystalline TiO_x films have been found ranging between 30 meV and 0.9 eV depending on the preparation method and oxidation structure of the TiO_x.[28,29]

These findings suggest that the gate leakage is controlled by a combination of all of these mechanisms dependent on the field and temperature of the device. At temperatures below 125 K and high E fields, J is dominated by Fowler-Nordheim tunneling through the triangular potential barrier. At similar temperatures and low E fields, trap assisted tunneling occurs in which the carriers find trap states in the dielectric before tunneling through the rest of the barrier. For all E and temperatures above 150 K, J is a combination of Poole-Frenkel tunneling and thermionic emission in which thermal excitation enhances the leakage current.

CONCLUSION

In summary, repeated cycles of PVD and oxidation of titanium was able to achieve high performance GFETs. We find that the Ti PVD layer is primarily oxidized *in situ* to TiO_2. By measuring a set of devices with different t_{ox}, we determine the dielectric constant of oxidized titanium to be κ = 6.9. Finally, we measured the leakage currents and investigated the possible conduction mechanisms in TiO_x gate dielectrics. While it is difficult to make definitive conclusions, we found evidence of Fowler-Nordheim tunneling at temperatures below 125 K and a combination of Poole-Frenkel tunneling and thermionic emission at temperatures above 125 K. This analysis suggests a conduction band edge barrier height of 0.78 eV and a trap depth of ∼45 meV below the conduction band.

MATERIALS AND METHODS

Dielectric Materials and Deposition. Titanium pellets better than 99.99% pure were placed in a titanium carbide crucible, both obtained from Kurt J. Lesker corporation. Films were deposited using an SEC-600 e-beam evaporator from CHA Industries. Films with a thickness of 10 Å were electron beam evaporated at a rate of less than 0.1 Å/s, at a starting pressure of 5×10^{-6} Torr background pressure, and then vented to atmosphere. During deposition, the pressure of the system drops to $\sim 1 \times 10^{-6}$ Torr and the exposure to atmosphere was less than 1 min when vented between repeated cycles; the maximum deposition temperature was 25 °C. *In situ* thickness measurements were obtained from a quartz crystal monitor.

Dielectric Thickness Characterization. Ellipsometry measurements were taken using a JJ Woollam M-2000 ellipsometer. Transmission electron micrographs were obtained with the FEI TECNAI G2 F20 X-TWIN system.

Transistor Fabrication. We mechanically exfoliated monolayer graphene layers on 285 nm thermally oxidized SiO_2 grown on highly doped n-type silicon.[30] Graphene monolayers are identified with a combination of Raman spectroscopy,[31] and optical contrast under white light.[32] We created the back-gated GFET channels with a combination of electron beam lithography (EBL) and oxygen plasma etching. After a subsequent EBL step to define contact regions, nickel was evaporated to form the source and drain. The GFETs were then annealed at 255 °C for 3 h at 9×10^{-9} Torr to remove process residues while preventing mobility degradation. We surmise the graphene comes into closer contact with the corrugated SiO_2 surface if annealed at temperatures higher than 275 °C, resulting in lower mobilities.[33] A set of GFETs were created using 2−10 cycles of Ti deposition and oxidation. A top gate was then defined by a subsequent EBL step and a nickel top gate electrode was deposited with electron beam evaporation and lift-off. For devices with thicker dielectrics, isolated contact windows were opened using a combination of EBL and CH_4 plasma.

Electrical Characterization. All electrical measurements were taken in a Lake Shore Cryotronics cryogenic probe station. All samples were measured in vacuum below 5×10^{-5} Torr and cooled with liquid nitrogen to achieve 77 K where stated. Data

was taken with an Agilent 4156C Semiconductor Parameter Analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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